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Enhanced Electrical Properties of Lithography-Free Fabricated MoS_2 Field Effect Transistors with Chromium Contacts

Hui Yang, Sa Cai, Yifei Zhang, Dongping Wu,* and Xiaosheng Fang*

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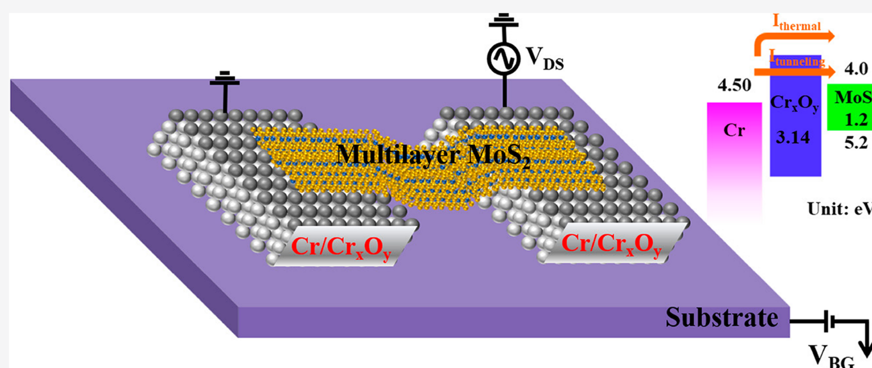

ABSTRACT: Molybdenum disulfide (MoS_2) as a two-dimensional semiconductor material has been actively explored for field-effect-transistors (FETs). The current prevailing method for MoS_2 FET fabrication involves multiple complex steps, including electron beam (e-beam) lithography, annealing, *etc.*, which are time-consuming and require polymer resists. As a consequence, the MoS_2 exposed to chemicals during the patterning process may be unfavorably affected by residues and the performance of the final FET could be impaired while the annealing limits materials for FETs. Therefore, there is an urgent need to free the fabrication of FETs from e-beam lithography and annealing. In this study, we introduce an e-beam lithography-free method to fabricate MoS_2 FETs by employing maze-like source/drain electrodes. In addition, an ohmic contact in multilayer MoS_2 FETs using chromium (Cr) as source/drain electrodes is achieved without annealing. The underlying mechanism for contact performance is studied, and the tightness of the contact and the type of metal are found to be responsible because they determine the contact resistance. Furthermore, the long-term device degradation is explored, in which the oxidation of metal dominates. The facile fabrication process and mechanism explanation in this work might provide a new platform for future electronic devices.

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Field effect transistors (FETs) based on two-dimensional (2D) thin films have attracted tremendous attention in recent years because they might enable next-generation nanoelectronic devices.[1−6] Molybdenum disulfide (MoS_2), one of layered transition-metal dichalcogenide materials held together by van der Waals interactions, is a particularly promising channel material in the fabrication of electronic and optoelectronic devices because of its high mobility, abrupt switching, large on/off current ratio, and immunity to short channel effects.[7−12] In addition, preliminary reports also indicate that MoS_2 FETs can be employed for sensing and energy-harvesting applications.[13−15]

To date, contacts of MoS_2 FETs are commonly fabricated through electron beam (e-beam) or photo lithography on top of MoS_2 flakes, both of which involve multiple wet processing steps where the residue of resists is often present on the surface of the MoS_2 flakes after device fabrication.[16] The resist residuals may unfavorably affect MoS_2 layer quality, thereby causing a significant variation in electrical performance of the MoS_2 FET.[17,18] To solve this problem, several approaches have been proposed, and among them, the lithography-free fabrication process is the most prevalent one.[19−25] Feng's group, for example, reported the use of a dry-transfer technique by transferring a preidentified MoS_2 flake to the designated location on the prepatterned substrate and obtained the desired device geometry.[26] As the FETs are fabricated by transferring MoS_2 flakes onto metal electrodes, the contact between metal electrodes and MoS_2 becomes one of the major performance-limiting factors for MoS_2 FETs. To improve the performance of MoS_2 FETs, an ohmic contact is desired at the interface to facilitate carrier transfer. Currently, methods to realize the ohmic contact mainly focus on increasing the

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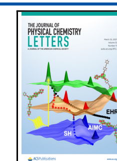

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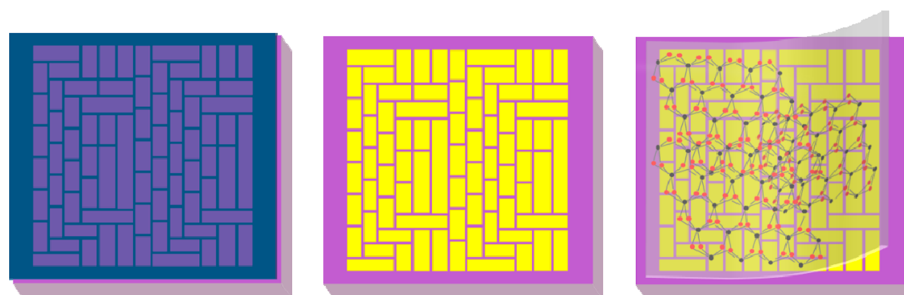

Figure 1. Schematic illustration of the MoS_2-based FETs fabrication process with maze-like source/drain electrode prepatterned wafer. (a) Patterned maze-like source/drain electrodes by photolithography, (b) deposition of the metal electrodes, and (c) mechanical exfoliation of MoS_2 flakes.

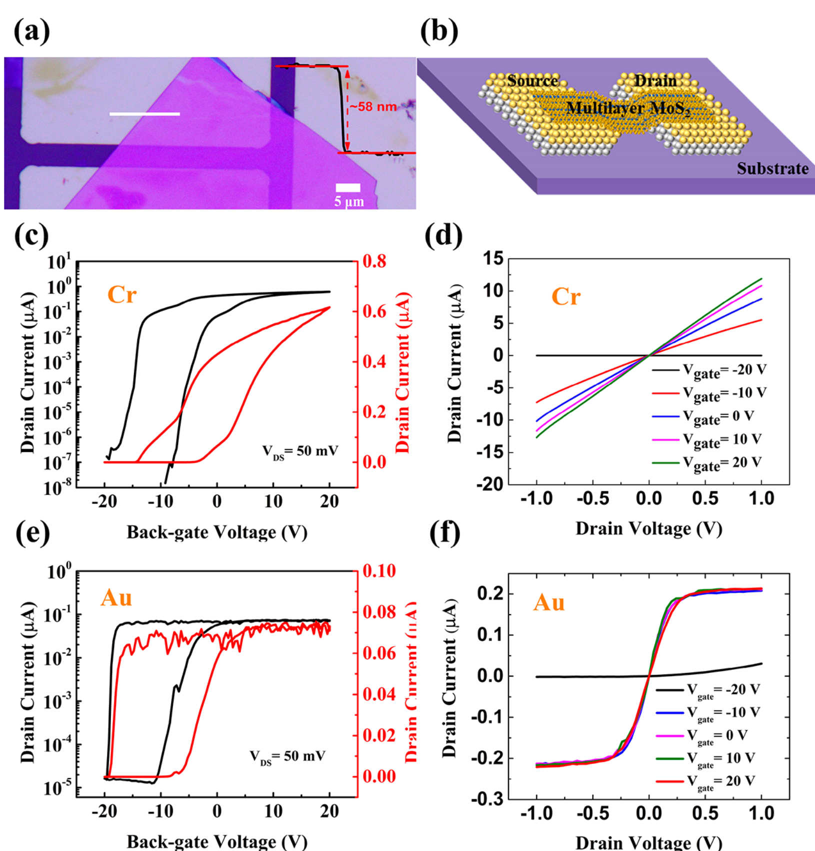

Figure 2. (a) Optical micrograph of a typical multilayer MoS_2 FET with Cr/Au (5 nm/50 nm) as source/drain electrodes. (b) Scheme of multilayer MoS_2 FET with Cr/Au (5 nm/50 nm) as source/drain electrodes. (c) Transfer curves of Cr-MoS_2 FET. (d) Output curves of Cr-MoS_2 FET. (e) Transfer curves of Au-MoS_2 FET. (f) Output curves of Au-MoS_2 FET.

interactions between metal electrode and MoS_2 by annealing,[26,27] whereas the electrode itself has been less studied.

Herein, we present a simple and e-beam lithography-free approach for the fabrication of multilayer MoS_2 FETs, which not only obviates the undesirable wet chemistry steps but also has a high device yield. Moreover, this approach could be potentially more scalable than the normal lithography methods currently used for MoS_2 electronic and optoelectronic devices. Furthermore, we found that ohmic contact was achieved directly without annealing treatment when chromium (Cr) was used as source/drain electrodes. Our study was complemented by comparing the results obtained from FETs with Au as source/drain electrodes. It was found that the quality of interface, especially intimate contact, played an important role in the formation of ohmic contact. We applied microwave annealing (MWA) to improve the contact of metal/MoS_2 interfaces to further confirm our conclusion, and results showed that MWA could significantly reduce the Schottky barrier at the MoS_2/Au interface. After MWA annealing at 840 W in nitrogen atmosphere, both the field effect mobility and on-state current of the FETs based on Au electrodes increased by 1−3 orders of magnitude.

In addition, the long-term performance of MoS_2 FET based on metallic Cr contact was studied, where a declined performance over time was observed. Analysis of the device performance and the metal thin film was conducted to explain the phenomenon. It was found that the rapid performance declination of MoS_2 FET mainly resulted from the thickness increase of Cr_xO_y.

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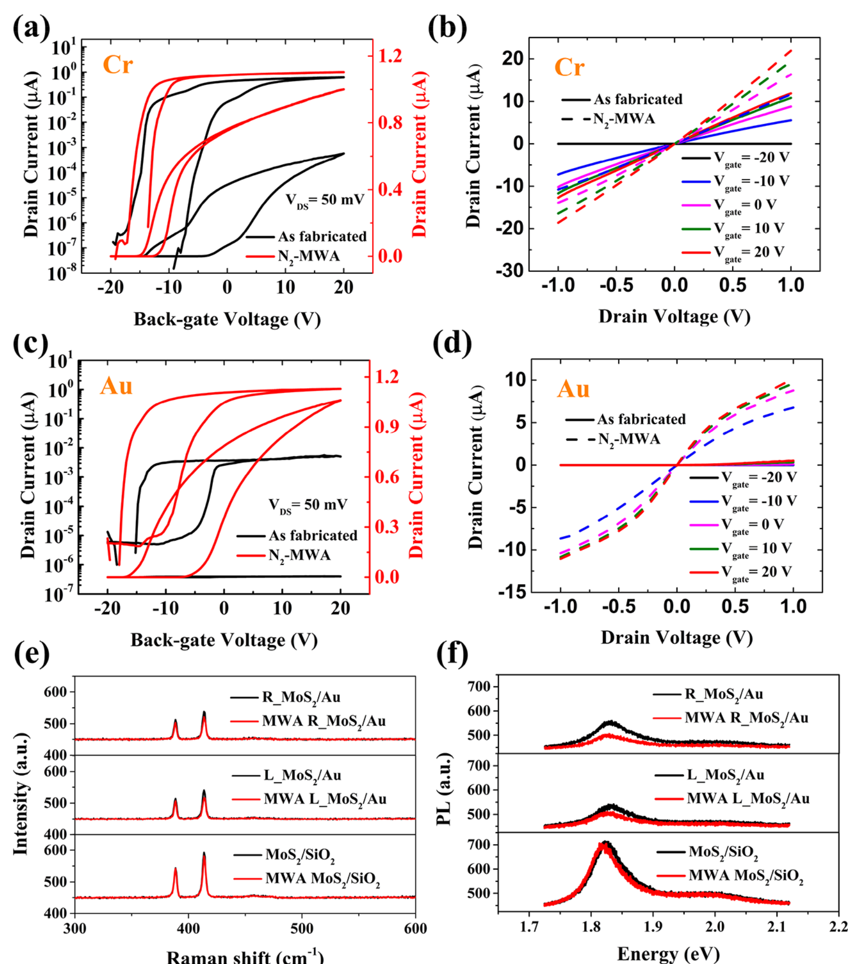

Figure 3. (a)Transfer curves of Cr-MoS_2 FET before and after MWA treatment. (b) Output curves of Cr-MoS_2 FET before and after MWA treatment. (c) Transfer curves of Au-MoS_2 FET before and after MWA treatment. (d) Output curves of Au-MoS_2 FET before and after MWA treatment. (e) Raman measurements for multilayer MoS_2 on SiO_2/Si substrate and on Au electrodes. (f) Photoluminescence (PL) measurements for multilayer MoS_2 on SiO_2/Si substrate and on Au electrodes.

Figure 1 shows the schematic diagram of fabrication processes of MoS_2-based FETs, including a pattern of maze-like electrodes by photolithography (Figure 1a), deposition of the metal electrodes (Figure 1b), and mechanical exfoliation of MoS_2 flakes (Figure 1c). The use of the maze-like source and drain structure can greatly improve the density of the source and drain electrodes in a unit area, thereby effectively improving the yield of fabricated devices. Suitable flakes with uniform thickness were selected by examining the contrast of color under an optical microscope (see the Supporting Information, Figure S1). In the present study, we mainly focused on devices based on MoS_2 thicker than 10 nm rather than few-layer or monolayer ones, because most reported devices used multilayer MoS_2 flakes as channel material.[28] Using this simple method, we fabricated MoS_2-based FETs and investigated the contact performance of mechanically exfoliated MoS_2 flakes with Cr and Au. The metal was grown by thermal evaporation (Nano-36 thermal evaporator, Kurt J. Lesker).

Figure 2a shows an optical image of a typical multilayer MoS_2 FET located on a 90 nm thin film of SiO_2 with heavily doped Si as the substrate, the film thickness was measured to be ~58 nm. The corresponding schematic structure of the multilayer MoS_2 FET is shown in Figure 2b. First, we studied the effect of Cr and Au as source/drain electrodes on the contact performance of the fabricated devices. Cr (20 nm) and a metal stack of Cr/Au (5 nm/50 nm) were used to fabricate the source/drain contacts employing photolithography. The transfer and output characteristics of multilayer MoS_2 FET made of Cr electrodes (Cr-MoS_2 FET) are presented in Figure 2c,d, and that of multilayer MoS_2 FET made of Cr/Au electrodes (Au-MoS_2 FET) are presented in Figure 2e,f. From Figure 2d,f, we can clearly see that an ohmic contact was realized when Cr was used as source/drain electrodes, while Au failed to form ohmic contact with multilayer MoS_2. Using the equation $\mu_{FE} = g_m L/(W C_{OX} V_{DS})$, where L, W, g_m, and C_{OX} are the channel length, width, transconductance, and gate capacitance at V_{DS} = 50 mV, respectively, the electric field mobility (μ_{FE}) of FET can be extracted. It was found that the μ_{FE} and on-state current (I_{ON}) of Cr-MoS_2 FETs were larger than that of Au-MoS_2 FETs. It is reasonable to presume that the higher mobility of Cr-MoS_2 FETs resulted from the low contact resistance at the MoS_2/Cr electrode interface, thus leading to a higher carrier injection efficiency. As e-beam lithography was not used in the device fabrication process, a clean channel and contact interface could be obtained. For both Cr-MoS_2 FETs and Au-MoS_2 FETs, the minimum subthreshold slopes (SS_{min}) of the device were at a very low level (see the Supporting Information, Figure S2). In order to explore the key factor in the formation of ohmic contact

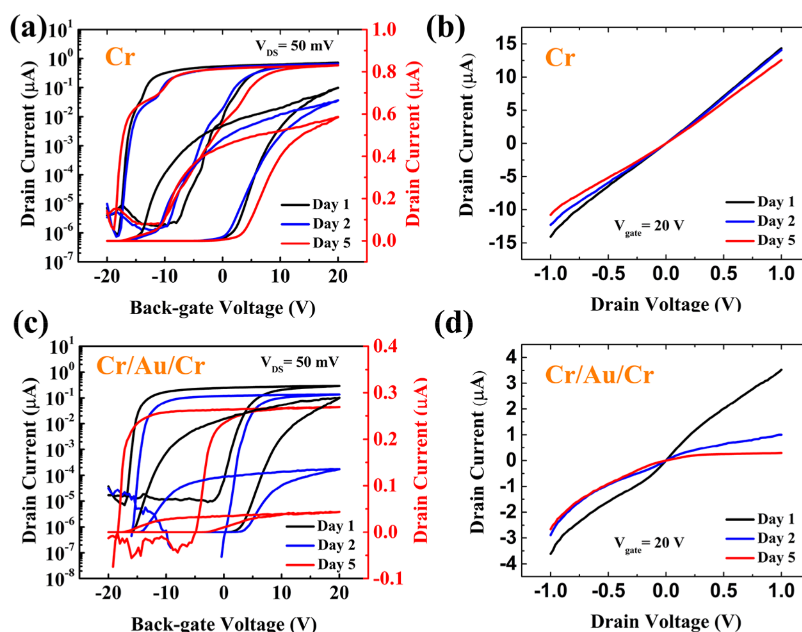

Figure 4. (a) Time dependence of transfer curves of MoS_2 FET using 20 nm Cr as source/drain electrodes. (b) Time dependence of output curves of MoS_2 FET using 20 nm Cr as source/drain electrodes. (c) Time dependence of transfer curves of MoS_2 FET using 5/15/20 nm Cr/Au/Cr as source/drain electrodes. (d) Time dependence of output curves of MoS_2 FET using 5/15/20 nm Cr/Au/Cr as source/drain electrodes.

between metal and multilayer MoS_2, a control experiment using liquid assisted exfoliation to fabricate MoS_2 FETs was conducted (see the Supporting Information, Figure S3). The multilayer MoS_2 fabricated from liquid-assisted exfoliation formed a more intimate contact with Au electrodes.[29] As shown in Figure S3b,c, this control multilayer Au-MoS_2 FET exhibited better transfer and output characteristics, indicating the reduced Schottky barrier. This revealed the importance of the intimate contact between multilayer MoS_2 and metal electrodes in the formation of the ohmic contact.

Annealing is widely adopted to improve the quality of contact between transition metal dichalcogenide (TMD) materials and metal as annealing can clean the TMD surface and subsequently induce intimate contact.[30−33] Here, we used microwave annealing (MWA) to investigate the effect of annealing on the contact performance of fabricated multilayer MoS_2 transistors. Referring to the process parameters of the MWA process from ref 34, the multilayer MoS_2 FETs were annealed in nitrogen atmosphere with 840 W power for 10 min. As shown in Figure 3a−d, the electrical performance of Au-MoS_2 FET was remarkably improved, while there was no significant performance improvement of Cr-MoS_2 FET. After annealing, both the field effect mobility and on-state current of the Au-MoS_2 FETs increased by 1−3 orders of magnitude (see the Supporting Information, Figure S4). The different effect of MWA on Cr-MoS_2 FET and Au-MoS_2 FET could further confirm that the contact between MoS_2 and Cr electrodes was more intimate than that between MoS_2 and Au electrodes; therefore, the MWA process could not significantly improve the electrical performance of the Cr-MoS_2 FET. For the Au-MoS_2 FET, the contact was not that intimate, and the MWA annealing effect was remarkable.

We further used photoluminescence (PL) and Raman spectroscopy to investigate the crystal quality of MoS_2 on top of the Au electrode and that on SiO_2/Si substrate before and after MWA.[27,35] The nearly identical PL and Raman peak intensities before and after annealing (Figure 3e,f) indicated that MWA did not change the intrinsic material properties of MoS_2 on SiO_2/Si substrate. In contrast, the decreased PL and Raman intensities of MoS_2 on Au electrodes after MWA revealed the property change. The possible cause for such difference could be the varied effect of MWA on the contact and substate.[36] For the relatively loose MoS_2/Au contact, MWA could make it significantly more intimate and increase the defect states of multilayer MoS_2, thus reducing the PL and Raman peak intensities.[37,38] For the multilayer and SiO_2/Si interface, MWA has little effect on improving it and the PL and Raman peak intensities showed little variation after annealing. From the above results, we could conclude that surface cleaning and intimate contact dominated the improvement of Au-MoS_2 FET performance. The great difference in the properties between Cr-MoS_2 FET and Au-MoS_2 FET might result from three possible causes: (1) A layer of natural chromium oxide (Cr_xO_y) was formed on the surface of Cr electrode in air, which helped to form a more intimate contact with molybdenum disulfide than Au.[39,40] (2) The lower work function of Cr reduced the Schottky barrier and contact resistance.[11] (3) The naturally formed very thin Cr_xO_y layer lowered the Fermi pinning effect of multilayer MoS_2.

Interestingly, an unusual attenuation of electrical performance of Cr-MoS_2 FETs was discovered during the experiments. The electrical performance of Cr-MoS_2 FET declined remarkably as time went by, and the decline rate was much higher than that of Au-MoS_2 FET. Previous studies have revealed that an ultrathin metal oxide insulator can reduce the Schottky barrier height (SBH), while further increasing the thickness of the insulator introduces a tunneling barrier that leads to the decrease of current.[41] In our experiment, there was a natural chromium oxide (Cr_xO_y) layer between Cr metal and MoS_2 film in the multilayer MoS_2 FET. Therefore, we proposed that it was the increasing thickness of Cr_xO_y over time that contributed to the rapid degradation of the electrical performance of Cr-MoS_2 FET. To validate our hypothesis, we prepared devices with two different metal electrodes: 20 nm Cr

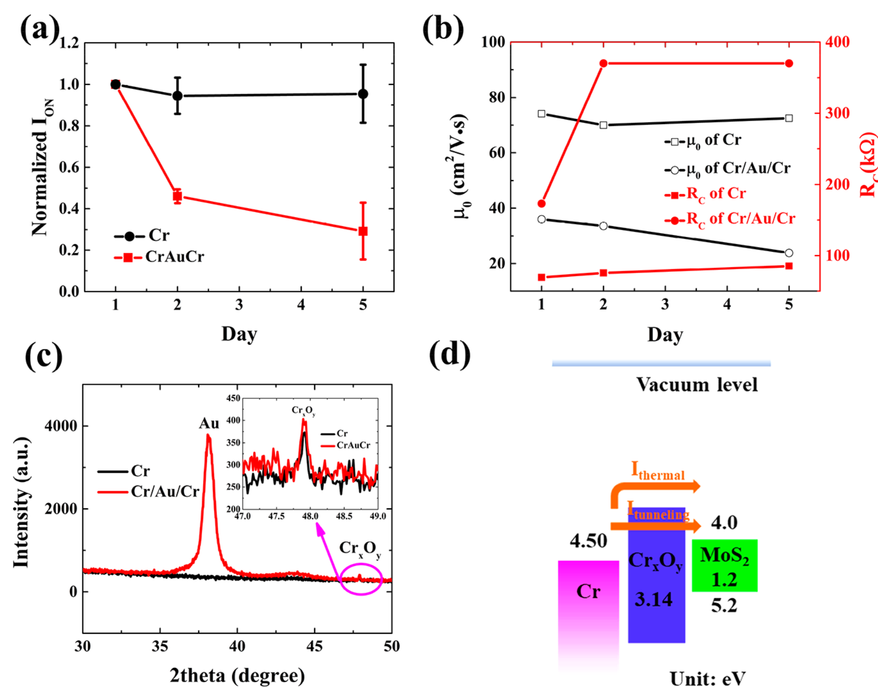

Figure 5. (a) Normalized on-state current (I_{ON}) of Cr-MoS_2 FETs and Cr/Au/Cr-MoS_2 FETs changing against time. Each set of data came from 3 separate MoS_2 FETs. (b) Time dependence of intrinsic mobility and contact resistance of Cr-MoS_2 FET and Cr/Au/Cr-MoS_2 FET. The electrical parameters of Cr-MoS_2 FET and Cr/Au/Cr-MoS_2 FET were extracted from the transfer curves of FETs in panels a and c of Figure 4, respectively. (c) XRD image of Cr and Cr/Au/Cr films on the fifth day. (d) Schematic energy band diagrams of a Cr/Cr_xO_y/MoS_2 structure. All band edge energies are with reference to vacuum; unit: eV.

electrode and 5/15/20 nm Cr/Au/Cr electrode. Figure 4 shows the electrical properties of Cr-MoS_2 FETs and Cr/Au/Cr-MoS_2 FETs in different time periods. It could be found that the degradation rate of electrical properties of Cr/Au/Cr-MoS_2 FETs was faster than that of Cr devices. Figure 5a shows the decay of the on-state current of the two contacts with time, and three FETs were tested for each electrode. It was obvious that the performance of Cr/Au/Cr-MoS_2 FETs declined faster. We also extracted the time-dependent relationship between the intrinsic mobility (μ_0) and contact resistance (R_C) of these two FETs in Figure 4 (for extraction methods of μ_0 and R_C, see note 1 of the Supporting Information).[42,43] The μ_0 of the FET decreased with time, indicating the declined film quality. However, this still could not explain the sharp decrease of the on-state current, and we further analyzed the contact resistance. The results showed that the R_C of Cr/Au/Cr-MoS_2 FET increased greatly during the next day and then remained relatively stable. However, the R_C of the Cr-MoS_2 FET increased stably for 5 days. We measured the XRD patterns of the Cr film and Cr/Au/Cr film prepared in the same batch of the FETs on the fifth day to determine the reason for the resistance variation. The results showed that the Cr_xO_y peak of Cr/Au/Cr film was stronger than that of Cr film on the fifth day. Therefore, we inferred that Cr on the surface of Au/Cr was easier to be oxidized, and the oxidation process was almost finished on the second day. We also tested the XRD patterns of these two films on day 8 (see the Supporting Information, Figure S5). The Cr_xO_y peak intensity of the two films was basically at the same level and was consistent with the peak intensity of Cr/Au/Cr film on the fifth day. Therefore, it was inferred that the Cr metal could reach a stable oxidation level after 8 days. As mentioned above, the existence of ultrathin Cr_xO_y could reduce gap states and provide a depinning effect, thus enhancing the electrical performance of multilayer MoS_2 FETs. However, a tunneling barrier would be introduced, and it would become the dominant component when the thickness of Cr_xO_y further increased with time (Figure 5d).[41,44] More work is still needed to compare Cr_xO_y with different thicknesses to further understand the depinning effect of Cr_xO_y/MoS_2 interface in the future.

In conclusion, we have demonstrated an e-beam lithography-free method to fabricate MoS_2 FET by employing maze-like source/drain electrodes. In addition, an ohmic contact was realized using Cr as source/drain electrodes, while Au failed to form ohmic contact with multilayer MoS_2. After MWA, the electrical performance of Au-MoS_2 FETs was remarkably improved, while there was no significant performance improvement of Cr-MoS_2 FETs. The great difference in the properties between Cr-MoS_2 FETs and Au-MoS_2 FETs might result from three possible aspects: (1) A layer of natural chromium oxide (Cr_xO_y) was formed on the surface of the Cr electrode in air, which helped to form a more intimate contact with molybdenum disulfide than Au. (2) The lower work function of Cr reduced the Schottky barrier and contact resistance. (3) The naturally formed very thin Cr_xO_y layer lowered the Fermi pinning effect of multilayer MoS_2. Furthermore, the long-term device degradation of the Cr-MoS_2 FET was explored, and we found it was the increasing thickness of Cr_xO_y over time that contributed to the rapid degradation of the electrical performance of Cr-MoS_2 FETs. The facile fabrication process and mechanism explanation in this work could offer a new efficient route toward high-quality MoS_2 FETs.

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■ ASSOCIATED CONTENT

Supporting Information

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Figures showing optical microscopy image of maze-like source/drain electrodes, statistics of Cr-MoS_2 FETs and Au-MoS_2 FETs in terms of μ_{FE} and SS_{min}, fabrication of Au-MoS_2 FETs using liquid-assisted exfoliation method and electrical performance of a typical Au-MoS_2 FET, statistics of Au-MoS_2 FETs before and after MWA in terms of μ_{FE} and I_{ON}, and XRD image of Cr and Cr/Au/Cr films on the eighth day; supplementary notes, including extraction of intrinsic mobility and contact resistance (PDF)

■ AUTHOR INFORMATION

Corresponding Authors

Dongping Wu − *State Key Laboratory of ASIC and System, Fudan University, Shanghai 200433, P.R. China*; Email: dongpingwu@fudan.edu.cn

Xiaosheng Fang − *Department of Materials Science, Fudan University, Shanghai 200433, P.R. China*; orcid.org/0000-0003-3387-4532; Email: xshfang@fudan.edu.cn

Authors

Hui Yang − *Department of Materials Science, Fudan University, Shanghai 200433, P.R. China*

Sa Cai − *Department of Materials Science, Fudan University, Shanghai 200433, P.R. China*

Yifei Zhang − *State Key Laboratory of ASIC and System, Fudan University, Shanghai 200433, P.R. China*

Complete contact information is available at: https://pubs.acs.org/10.1021/acs.jpclett.1c00231

Notes

The authors declare no competing financial interest.

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■ REFERENCES

(1) Novoselov, K. S.; Jiang, D.; Schedin, F.; Booth, T. J.; Khotkevich, V. V.; Morozov, S. V.; Geim, A. K. Two-Dimensional Atomic Crystals. *Proc. Natl. Acad. Sci. U. S. A.* **2005**, *102*, 10451−10453.

(2) Li, S. Y.; Zhang, Y.; Yang, W.; Liu, H.; Fang, X. S. 2D Perovskite $Sr_2Nb_3O_{10}$ for High-Performance UV Photodetectors. *Adv. Mater.* **2020**, *32*, 1905443.

(3) Wang, H.; Yu, L. L.; Lee, Y. H.; Shi, Y. M.; Hsu, A.; Chin, M. L.; Li, L. J.; Dubey, M.; Kong, J.; Palacios, T. Integrated Circuits Based on Bilayer MoS_2 Transistors. *Nano Lett.* **2012**, *12*, 4674−4680.

(4) Chhowalla, M.; Shin, H. S.; Eda, G.; Li, L. J.; Loh, K. P.; Zhang, H. The Chemistry of Two-Dimensional Layered Transition Metal Dichalcogenide Nanosheets. *Nat. Chem.* **2013**, *5*, 263−275.

(5) Wang, H. P.; Li, S. Y.; Liu, X. Y.; Shi, Z. F.; Fang, X. S.; He, J. H. Low-Dimensional Metal Halide Perovskite Photodetectors. *Adv. Mater.* **2021**, *33*, 2003309.

(6) Li, L. K.; Yu, Y. J.; Ye, G. J.; Ge, Q. Q.; Ou, X. D.; Wu, H.; Feng, D. L.; Chen, X. H.; Zhang, Y. B. Black Phosphorous Field-Effect Transistors. *Nat. Nanotechnol.* **2014**, *9*, 372−377.

(7) Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-Layer MoS_2 Transistors. *Nat. Nanotechnol.* **2011**, *6*, 147−150.

(8) Yoon, Y.; Ganapathi, K.; Salahuddin, S. How Good Can Monolayer MoS_2 Transistors Be? *Nano Lett.* **2011**, *11*, 3768−3773.

(9) Yin, Z. Y.; Li, H.; Jiang, L.; Shi, Y. M.; Sun, Y. H.; Lu, G.; Zhang, Q.; Chen, X. D.; Zhang, H. Single-Layer MoS_2 Phototransistors. *ACS Nano* **2012**, *6*, 74−80.

(10) Kim, S.; Konar, A.; Hwang, W. S.; Lee, J. H.; Lee, J.; Yang, J.; Jung, C.; Kim, H.; Yoo, J. B.; Choi, J. Y.; Jin, Y. W.; Lee, S. Y.; Jena, D.; Choi, W.; Kim, K. High-Mobility and Low-Power Thin Film Transistors Based on Multilayer MoS_2 Crystals. *Nat. Commun.* **2012**, *3*, 1011.

(11) Das, S.; Chen, H. Y.; Penumatcha, A. V.; Appenzeller, J. High Performance Multilayer MoS_2 Transistors with Scandium Contacts. *Nano Lett.* **2013**, *13*, 100−105.

(12) English, C. D.; Shine, G.; Dorgan, V. E.; Saraswat, K. C.; Pop, E. Improved Contacts to MoS_2 Transistors by Ultra-High Vacuum Metal Deposition. *Nano Lett.* **2016**, *16*, 3824−3830.

(13) Li, H.; Yin, Z. Y.; He, Q. Y.; Li, H.; Huang, X.; Lu, G.; Fam, D. W. H.; Tok, A. I. Y.; Zhang, Q.; Zhang, H. Fabrication of Single- and Multilayer MoS_2 Film-Based Field-Effect Transistors for Sensing NO at Room Temperature. *Small* **2012**, *8*, 63−67.

(14) Wu, C. C.; Jariwala, D.; Sangwan, V. K.; Marks, T. J.; Hersam, M. C.; Lauhon, L. J. Elucidating the Photoresponse of Ultrathin MoS_2 Field-Effect Transistor by Scanning Photocurrent Microscopy. *J. Phys. Chem. Lett.* **2013**, *4*, 2508−2513.

(15) Zhang, X.; Grajal, J.; Vazquez-Roy, J. L.; Radhakrishna, U.; Wang, X. X.; Chern, W.; Zhou, L.; Lin, Y. X.; Shen, P. C.; Ji, X.; Ling, X.; Zubair, A.; Zhang, Y. H.; Wang, H.; Dubey, M.; Kong, J.; Dresselhaus, M.; Palacios, T. Two-Dimensional MoS_2-Enabled Rectenna for Wi-Fi-Band Wireless Energy Harvesting. *Nature* **2019**, *566*, 368.

(16) Liang, J. R.; Xu, K.; Toncini, B.; Bersch, B.; Jariwala, B.; Lin, Y. C.; Robinson, J.; Fullerton-Shirey, S. K. Impact of Post-Lithography Polymer Residue on the Electrical Characteristics of MoS_2 and WSe_2 Field Effect Transistors. *Adv. Mater. Interfaces* **2019**, *6*, 1801321.

(17) Zhao, J.; Yu, H.; Chen, W.; Yang, R.; Zhu, J. Q.; Liao, M. Z.; Shi, D. X.; Zhang, G. Y. Patterned Peeling 2D MoS_2 off the Substrate. *ACS Appl. Mater. Interfaces* **2016**, *8*, 16546−16550.

(18) Woo, G.; Kim, H. U.; Yoo, H.; Kim, T. Recyclable Free-Polymer Transfer of Nano-Grain MoS_2 Film onto Arbitrary Substrates. *Nanotechnology* **2021**, *32*, 045702.

(19) Bao, W. Z.; Liu, G.; Zhao, Z.; Zhang, H.; Yan, D.; Deshpande, A.; Leroy, B. J.; Lau, C. N. Lithography-Free Fabrication of High Quality Substrate-Supported and Freestanding Graphene Devices. *Nano Res.* **2010**, *3*, 98−102.

(20) Geringer, V.; Subramaniam, D.; Michel, A. K.; Szafranek, B.; Schall, D.; Georgi, A.; Mashoff, T.; Neumaier, D.; Liebmann, M.; Morgenstern, M. Electrical Transport and Low-Temperature Scanning Tunneling Microscopy of Microsoldered Graphene. *Appl. Phys. Lett.* **2010**, *96*, 082114.

(21) Tien, D. H.; Park, J. Y.; Kim, K. B.; Lee, N.; Seo, Y. Characterization of Graphene-Based FET Fabricated Using a Shadow Mask. *Sci. Rep.* **2016**, *6*, 25050.

(22) Chen, X.; Park, Y. J.; Das, T.; Jang, H.; Lee, J. B.; Ahn, J. H. Lithography-Free Plasma-Induced Patterned Growth of MoS_2 and Its Heterojunction with Graphene. *Nanoscale* **2016**, *8*, 15181−15188.

(23) Gant, P.; Niu, Y.; Svatek, S. A.; Agrait, N.; Munuera, C.; Garcia-hernandez, M.; Frisenda, R.; de Lara, D. P.; Castellanos-Gomez, A. Lithography-Free Electrical Transport Measurements on 2D Materials by Direct Microprobing. *J. Mater. Chem. C* **2017**, *5*, 11252−11258.

(24) Yoo, S.; Kim, S.; Song, Y. W. Lithography-Free Fabrication of Field Effect Transistor Channels with Randomly Contact-Printed Black Phosphorus Flakes. *Mater. Sci. Semicond. Process.* **2018**, *86*, 58−62.

(25) Li, Z. Q.; Li, Z. L.; Shi, Z. F.; Fang, X. S. Facet-dependent, Fast Response, and Broadband Photodetector based on Highly Stable All-inorganic $CsCu_2I_3$ Single Crystal with 1D Electronic Structure. *Adv. Funct. Mater.* **2020**, *30*, 2002634.
(26) Yang, R.; Zheng, X. Q.; Wang, Z. H.; Miller, C. J.; Feng, P. X. L. Multilayer MoS_2 Transistors Enabled by a Facile Dry-Transfer Technique and Thermal Annealing. *J. Vac. Sci. Technol., B: Nanotechnol. Microelectron.: Mater., Process., Meas., Phenom.* **2014**, *32*, 061203.
(27) Islam, A.; Lee, J.; Feng, P. X. L. All-Dry Transferred Single- and Few-Layer MoS_2 Field Effect Transistor with Enhanced Performance by Thermal Annealing. *J. Appl. Phys.* **2018**, *123*, 025701.
(28) Kim, S.; Konar, A.; Hwang, W. S.; Lee, J. H.; Lee, J.; Yang, J.; Jung, C.; Kim, H.; Yoo, J. B.; Choi, J. Y.; Jin, Y. W.; Lee, S. Y.; Jena, D.; Choi, W.; Kim, K. High-Mobility and Low-Power Thin-Film Transistors Based on Multilayer MoS_2 Crystals. *Nat. Commun.* **2012**, *3*, 1011.
(29) Liu, X. Y.; Huang, K. L.; Zhao, M.; Li, F.; Liu, H. G. A Modified Wrinkle-Free MoS_2 Film Transfer Method for Large Area High Mobility Field-Effect Transistor. *Nanotechnology* **2020**, *31*, 055707.
(30) Heinze, S.; Tersoff, J.; Martel, R.; Derycke, V.; Appenzeller, J.; Avouris, P. H. Carbon Nanotubes as Schottky Barrier Transistors. *Phys. Rev. Lett.* **2002**, *89*, 106801.
(31) Cheng, Z. G.; Zhou, Q. Y.; Wang, C. X.; Li, Q. A.; Wang, C.; Fang, Y. Toward Intrinsic Graphene Surfaces: A Systematic Study on Thermal Annealing and Wet-Chemical Treatment of SiO_2-Supported Graphene Devices. *Nano Lett.* **2011**, *11*, 767−771.
(32) Bolshakov, P.; Zhao, P.; Azcatl, A.; Hurley, P. K.; Wallace, R. M.; Young, C. D. Improvement in Top-Gate MoS_2 Transistor Performance Due to High Quality Backside Al_2O_3 Layer. *Appl. Phys. Lett.* **2017**, *111*, 032110.
(33) Qi, D. Y.; Wang, Q. X.; Han, C.; Jiang, J. Z.; Zheng, Y. J.; Chen, W.; Zhang, W. J.; Wee, A. T. S. Reducing the Schottky Barrier between Few-Layer $MoTe_2$ and Gold. *2D Mater.* **2017**, *4*, 045016.
(34) Yang, H.; Li, C.; Yue, L.; Wen, C. Y.; Zhang, J. K.; Wu, D. P. Improving Electrical Performance of Few-Layer MoS_2 FETs via Microwave Annealing. *IEEE Electron Device Lett.* **2019**, *40*, 1116−1119.
(35) Chen, F.; Wang, L.; Wang, T.; Ji, X. H. Enhanced Local Photoluminescence of a Multilayer MoS_2 Nanodot Stacked on Monolayer MoS_2 Flakes. *Opt. Mater. Express* **2017**, *7*, 1365−1373.
(36) Ko, C. J.; Lin, Y. K.; Chen, F. C. Microwave Annealing of Polymer Photovoltaic Devices. *Adv. Mater.* **2007**, *19*, 3520−3523.
(37) Golovynskyi, S.; Irfan, I.; Bosi, M.; Seravalli, L.; Datsenko, O. I.; Golovynska, I.; Li, B. K.; Lin, D. Y.; Qu, J. L. Exciton and Trion in Few-Layer MoS_2: Thickness and Temperature-Dependent Photoluminescence. *Appl. Surf. Sci.* **2020**, *515*, 146033.
(38) Wang, X. W.; Fan, W.; Fan, Z. W.; Dai, W. Y.; Zhu, K. L.; Hong, S. Z.; Sun, Y. F.; Wu, J. Q.; Liu, K. Substrate Modified Thermal Stability of Mono- and Few-Layer MoS_2. *Nanoscale* **2018**, *10*, 3540−3546.
(39) Ahmed, F.; Choi, M. S.; Liu, X.; Yoo, W. J. Carrier Transport at the Metal-MoS_2 Interface. *Nanoscale* **2015**, *7*, 9222−9228.
(40) Smyth, C. M.; Addou, R.; McDonnell, S.; Hinkle, C. L.; Wallace, R. M. Contact Metal-MoS_2 Interfacial Reactions and Potential Implications on MoS_2-Based Device Performance. *J. Phys. Chem. C* **2016**, *120*, 14719−14729.
(41) Zheng, S.; Lu, H. C.; Liu, H.; Liu, D. M.; Robertson, J. Insertion of an Ultrathin Al_2O_3 Interfacial Layer for Schottky Barrier Height Reduction in WS_2 Field-Effect Transistors. *Nanoscale* **2019**, *11*, 4811−4821.
(42) Chang, H. Y.; Zhu, W. N.; Akinwande, D. On the Mobility and Contact Resistance Evaluation for Transistors Based on MoS_2 or Two-Dimensional Semiconducting Atomic Crystals. *Appl. Phys. Lett.* **2014**, *104*, 113504.
(43) Bhattacharjee, S.; Ganapathi, K. L.; Nath, D. N.; Bhat, N. Intrinsic Limit for Contact Resistance in Exfoliated Multilayered MoS_2 FET. *IEEE Electron Device Lett.* **2016**, *37*, 119−122.
(44) Greiner, M. T.; Lu, Z. H. Thin-Film Metal Oxides in Organic Semiconductor Devices: Their Electronic Structures, Work Functions and Interfaces. *NPG Asia Mater.* **2013**, *5*, No. e55.