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Low-Power Optoelectronic Hybrid Perovskite-Based Memristor for Ternary Hardware Security Monitoring

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Secure intelligent electronics with high integration and adaptability are critical for next-generation information systems. However, previously reported hardware systems typically employ separate sensing, memory, and processing modules, leading to increased system complexity, high latency, and energy inefficiency. Here, high-quality hybrid perovskite nanoplates are synthesized and utilized to construct optoelectronic memristors. The device exhibits broadband self-powered photodetection and reliable resistive switching, with a remarkably low setting power (≈1.21 pW) and an ultra-high on/off ratio (≈10^6). By leveraging optically and electrically programmed states, the device enables reconfigurable access control and real-time security monitoring within a 3 × 3 array. The implementation of ternary logic states enables both spatially and state-dependent access patterns with an ultra-low write energy (≈3.8 f)/bit). The device achieves higher information density and enhanced hardware security monitoring without the need for additional logic circuits, offering strong potential for secure access management, intelligent sensor networks, and energy-efficient multifunctional electronics.

1. Introduction

With the rapid growth of the Internet of Things (IoT) and artificial intelligence (AI), ensuring secure and reliable device operation has become a critical concern. As numerous IoT nodes and edge devices operate in unregulated environments, traditional hardware solutions including physically unclonable functions,[1,2] true random number generators,[3,4] logic operations,[5] and information hiding techniques[6] exhibit inherent limitations including limited reconfigurability, the need for dedicated circuitry, complex algorithmic architectures, functional singularity, inflexibility, and reliance on external carriers. Therefore, integrating physical entropy, reconfigurable input schemes, versatile signal processing, and high information density within a unified architecture is emerging as a major trend in advanced security electronics.

Dual-functional devices that integrate sensing and memory within a single platform can streamline information processing by minimizing inter-module data transfer, thereby reducing system latency and improving energy efficiency. Such devices have been increasingly reported in various application domains, including neuromorphic systems, edge computing, smart sensor networks, biomedical health monitoring, and environmental sensing. A range of material systems has been applied in dual-functional devices, including metal oxides,[7,8] polymers,[9] traditional 2D materials,[10,11] perovskites,[12,13] and their composites.[14,15] However, these systems still face limitations, including processing complexity and limited endurance or retention. Therefore, there remains a strong need for alternative material systems that can provide stable, reconfigurable, and scalable performance under various inputs.

Hybrid perovskites, endowed with excellent optoelectronic properties and high power conversion efficiency, show great potential in photovoltaics,[16,17] LEDs,[18,19] photodetectors,[20,21] resistive random-access memory (RRAM),[22,23] optoelectronic memory/computing,[24] and other applications. In particular, 2D Ruddlesden–Popper (RP) hybrid perovskites have garnered significant attention due to their unique layered structures, enhanced environmental stability, and tunable optoelectronic properties.[25,26] Compared to 3D perovskites, RP-phase perovskites offer higher defect formation energies and enhanced environmental stability, making them better suited for low-power and robust memristor devices.[27,28] Although Dion–Jacobson (DJ) perovskites feature strong interlayer connections and lack van der Waals gaps, their complex processing and poor solubility limit scalability.[29–31] Specifically, a high-performance ultraviolet photodetector based on PA_2PbBr_4 perovskite enabled high-resolution imaging under low-light conditions.[32] A $BA_2MA_3Pb_4Br_{13}$ perovskite-based ferroelectric memristor was developed to mimic synaptic plasticity, providing a versatile platform for artificial vision and neuromorphic computing.[33] However, the potential of RP perovskite-based dual-functional devices that combine optical sensing and electrical memory for multifunctional hardware applications remains underexplored.

In this study, we synthesize high-quality hybrid $PEA_2MA_{n-1}Pb_nI_{3n+1}$ perovskite nanoplates characterized by excellent uniformity and crystallinity. Utilizing the nanoplates, we develop an Ag/PMMA/$PEA_2MAPb_2I_7$/ITO optoelectronic memristor integrating broadband self-powered photodetection with resistive switching functionality. The device features a

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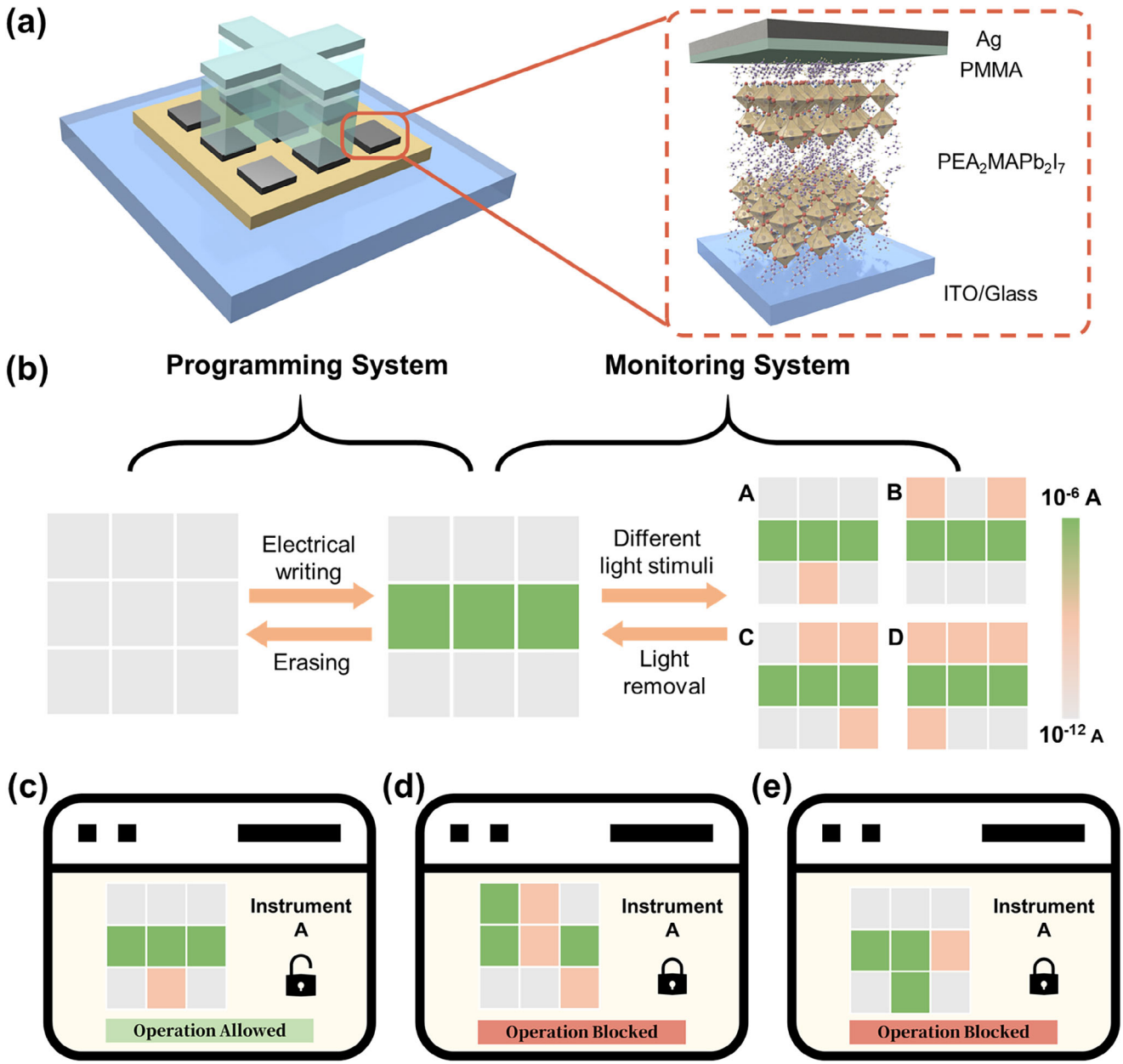

Figure 1. Working mechanism for photonic–electronic access control. a) Schematic diagram of the dual-functional device, presenting a regular 3 × 3 array and an enlarged view of a single Ag/PMMA/$PEA_2MAPb_2I_7$/ITO device unit. b) The dual-factor input patterns, including a static access code set by electrical programming (green) and real-time optical activation (orange) at different positions. c) Operation is allowed when optical and electrical patterns match and form a valid key. d) Operation is blocked due to incorrect optical input. e) Operation is blocked due to a misconfigured electrical state.

large photoresponsivity (39.1 mA/W) and a high detectivity (1.15×10^{11} Jones), while exhibiting excellent programmable performance with a low operating voltage (0.44 V), an ultra-low setting power (≈1.21 pW), an ultra-high on/off ratio (≈10^6), high endurance (>100 cycles), and programmable retention time (>1.6×10^4 s). By leveraging ternary state encoding in both spatial and physical dimensions, the system achieves an ultra-low write energy (≈3.8 fJ/bit), indicating strong potential for multifunctional and scalable hardware applications.

2. Results and Discussion

2.1. Working Mechanism for Photonic–Electronic Access Control

Figure 1 illustrates the operating principle of the fabricated optoelectronic memristor for security monitoring applications. The schematic diagram of the device structure is shown in Figure 1a. Each unit in a 3 × 3 array for information tracking consists of Ag/PMMA/$PEA_2MAPb_2I_7$/ITO layers on a glass substrate. The detailed layout of the device components reveals that Ag serves

as a top electrode, poly(methyl methacrylate) (PMMA) acts as a passivation layer to suppress dark current,[34] $PEA_2MAPb_2I_7$ nanoplate enables both photoconductive and memristive behavior, and indium tin oxide (ITO) functions as the bottom electrode.

The dual-factor security monitoring operation is achieved by combining electrical programming with optically triggered verification (Figure 1b). A 0.2 V read bias is used to track the device state. Initially, the device is in a neutral high-resistance state (HRS), corresponding to a baseline current level of $\approx 10^{-12}$ A. When electrical stimuli exceeding the setting voltage are applied to the central row of the array, the selected units respond with resistive switching behavior and transform from the initial HRS to a low-resistance state (LRS, $\approx 10^{-6}$ A). The LRS remains stable after the stimulation, thereby storing the static access code. Alternatively, the optical input functions asa dynamic signal. When the light stimuli are applied to specific patterns or positions of the array as determined by the instrument being accessed, the corresponding cells capture the optical signals and generate a transient photocurrent from $\approx 10^{-12}$ A to $\approx 10^{-9}$ A, indicating the formation of a temporary conductive state. With the removal of illumination, the photoconductive state rapidly reverts to the original HRS, ensuring active monitoring.

Figure 1c–e illustrates the access control process under different input conditions. As shown in Figure 1c, operation is allowed only when the real-time optical monitoring pattern fully overlaps with the electrically programmed static pattern to form the predefined ternary key. Any mismatch caused by either misalignment of activation or incorrect configuration of the static memory states results in the operation being blocked. Figure 1d shows a representative scenario in which operation is blocked due to the optical and electrical activation patterns deviating from the expected configuration. Although the visual pattern formed by optical stimulation appears identical to the target key, the underlying electrical states do not correspond to the required programmed configuration, which results in the operation being blocked (Figure 1e). Unlike conventional approaches based solely on pattern or visual matching, our dual-functional device enforces the concurrent agreement of both optical and electrical states, thereby greatly enhancing the robustness and security of operation control at the hardware level.

2.2. Fundamental Characterizations of Hybrid Perovskites

The fundamental characterizations of $PEA_2MA_{n-1}Pb_nI_{3n+1}$ hybrid perovskites are demonstrated in **Figure 2**. As illustrated in Figure S1 (Supporting Information), hybrid $PEA_2MA_{n-1}Pb_nI_{3n+1}$ perovskite nanoplates synthesized by the liquid–air interface floating growth method are uniformly distributed.[35,36] The low-magnification optical image shows that the nanoplates are uniformly distributed over a large area and exhibit various polygonal morphologies. To quantify its uniformity, we statistically analyzed 22 nanoplates captured in a single optical micrograph, yielding a lateral size of 36.91 ± 6.89 µm (mean ± standard deviation), which is beneficial for reproducible material synthesis. Optical microscopy images of the nanoplates with different layer numbers (n = 1–4) are also provided in Figure S2 (Supporting Information), demonstrating their uniform morphology across varying compositions. The size of the nanoplates can be regulated by the duration of the growth at the liquid–air interface. Crystal growth preferentially occurs at the droplet surface, where reduced confinement and higher atomic mobility lower the nucleation barrier, facilitating the formation and expansion of the nanoplate (Figure S3, Supporting Information).[37] As the crystallization time increases from 30 s to 300 s, the surface area increases from 5.85×10^{-4} mm^2 to 7.16×10^{-2} mm^2 (Figure S4, Supporting Information). The PDMS stamping process yields clean, defect-free interfaces and preserves the intrinsic quality of the perovskite nanoplates. AFM image of the ITO/glass substrates (Figure S5, Supporting Information) confirms low roughness and high flatness, indicating that the transfer does not compromise the quality or reliability. The AFM image of $PEA_2MAPb_2I_7$ ($n = 2$) nanoplate reveals a well-defined layered surface with a thickness of 43.3 nm and the surface roughness (R_q) of 4.16 nm (Figure 2a). The $n = 1$ nanoplate also exhibits a smooth and ordered surface morphology on the ITO substrate (Figure S6, Supporting Information). As shown in Figure 2b, the high-resolution TEM (HRTEM) image of $n = 2$ nanoplate reveals clear lattice fringes and an ordered atomic arrangement between adjacent planes, confirming high crystallinity. The measured interplanar spacing is 2.3 Å, corresponding to the (0200) crystal plane of the nanoplates. A schematic diagram for calculating the crystal plane spacing is provided in Figure S7 (Supporting Information). The inset shows the associated fast Fourier transform (FFT) pattern, further supporting its high-quality crystalline structure. The selected area electron diffraction (SAED) pattern in Figure 2c displays strong reflections and clear diffraction spots, being indexed to the (0120) and (2−1−1) planes, confirming the high crystallinity of the sample. Figure 2d shows the SEM and the corresponding inset optical images of the nanoplate, exhibiting a good morphology and a flat surface. Corresponding energy dispersive X-ray spectroscopy (EDS) elemental mappings (Figure 2e) indicate that C, N, I, and Pb are homogeneously distributed in the nanoplate. SEM images of the n = 1, 3, and 4 nanoplates are also provided in Figure S8 (Supporting Information), all showing uniform shapes and smooth surfaces.

Structural analysis was performed to reveal the atomic arrangement. Figure 2f illustrates the crystal structure of the n = 2 perovskite, showing alternating organic and inorganic layers with corner-sharing $[PbI_6]^{4-}$ octahedra. The XRD pattern of n = 2 perovskite is shown in Figure 2g, indicating that the diffraction pattern for the perovskite has nine broad peaks at 7.8°, 11.7°, 15.7°,19.6°, 23.6°, 27.6°, 31.7°, 35.7°, and 39.9°, corresponding to (040), (060), (080), (0100), (0120), (0140), (0160), (0180), and (0200) facets. Figure S9 (Supporting Information) displays the diffraction pattern of the n = 1 perovskite showing a series of peaks including (002), (004), (006), (008), (0010), and (0012), confirming a similarly well-ordered layered structure. The photoluminescence (PL) spectra of $PEA_2MA_{n-1}Pb_nI_{3n+1}$ of n = 1–4 exhibit a distinct emission peak at 522 nm, 577 nm, 622 nm, and 775 nm, respectively, indicating a gradual redshift in emission with increasing layer number (Figure 2h). The corresponding band gaps are 2.38, 2.15, 1.99, and 1.60 eV using the formula $E_g = hc/\lambda$, where h is Planck's constant, c is the speed of light, and λ is the emission wavelength. XPS was employed to examine the chemical states of the constituent elements. As shown in Figure S10 (Supporting Information), the XPS survey spectrum confirms the presence of C, N, I, and Pb in the $n = 2$ nanoplates,

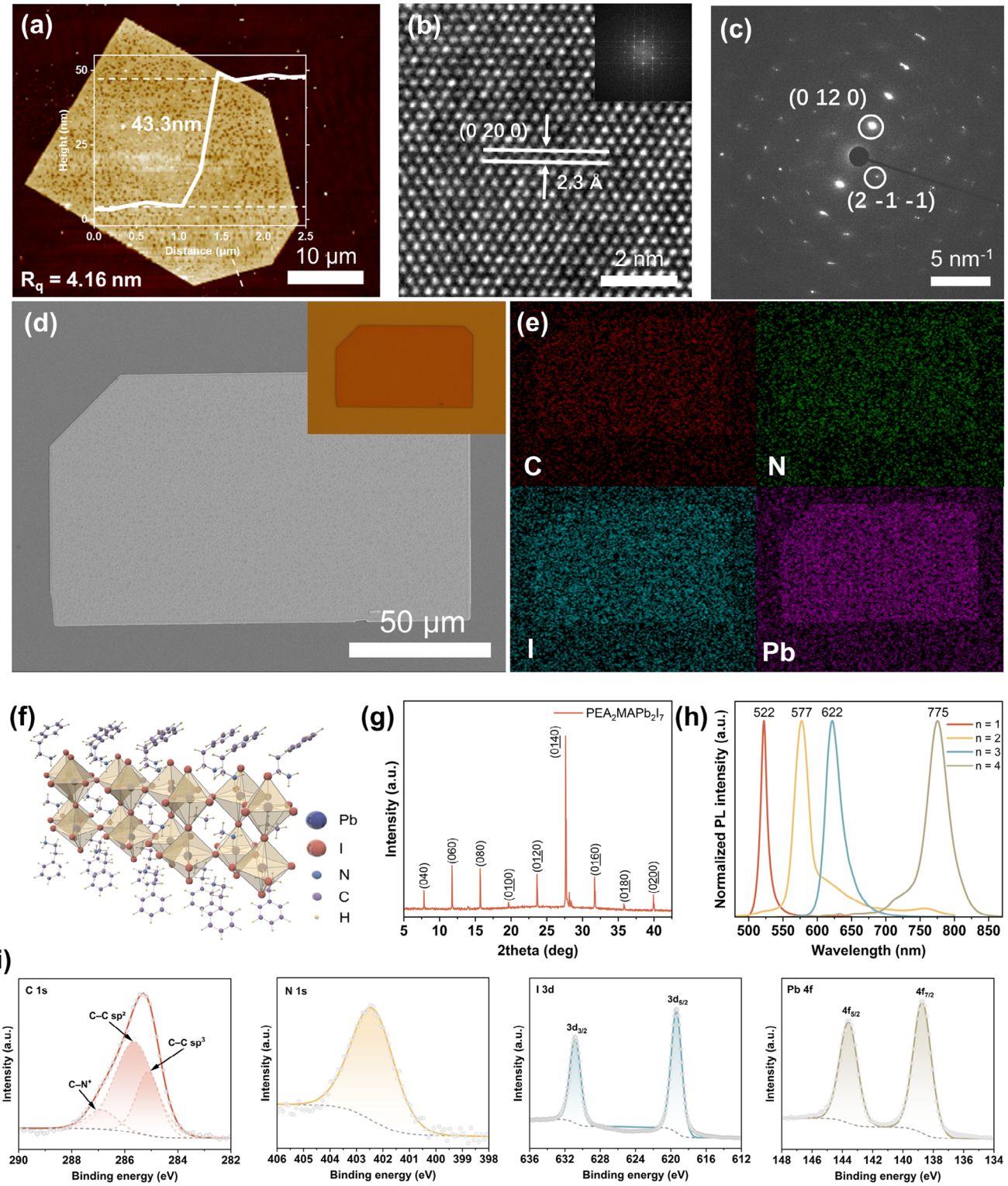

Figure 2. Fundamental characterizations of hybrid perovskites. a) AFM image of the $PEA_2MAPb_2I_7$ nanoplate surface structure. b) HRTEM image and corresponding FFT pattern (inset) of the $PEA_2MAPb_2I_7$ nanoplate. c) SAED pattern of the $PEA_2MAPb_2I_7$ nanoplate. d) SEM image and optical image (inset) of the $PEA_2MAPb_2I_7$ nanoplate. e) EDS mappings showing the distribution of C, N, I, and Pb elements. f) Structural schematic of $PEA_2MAPb_2I_7$ crystal. g) XRD pattern of $PEA_2MAPb_2I_7$ structure. h) PL spectra of $PEA_2MA_{n-1}Pb_nI_{3n+1}$ crystal with varying n. i) High-resolution XPS spectra of C 1s, N 1s, I 3d, and Pb 4f regions in the $PEA_2MAPb_2I_7$ crystal.

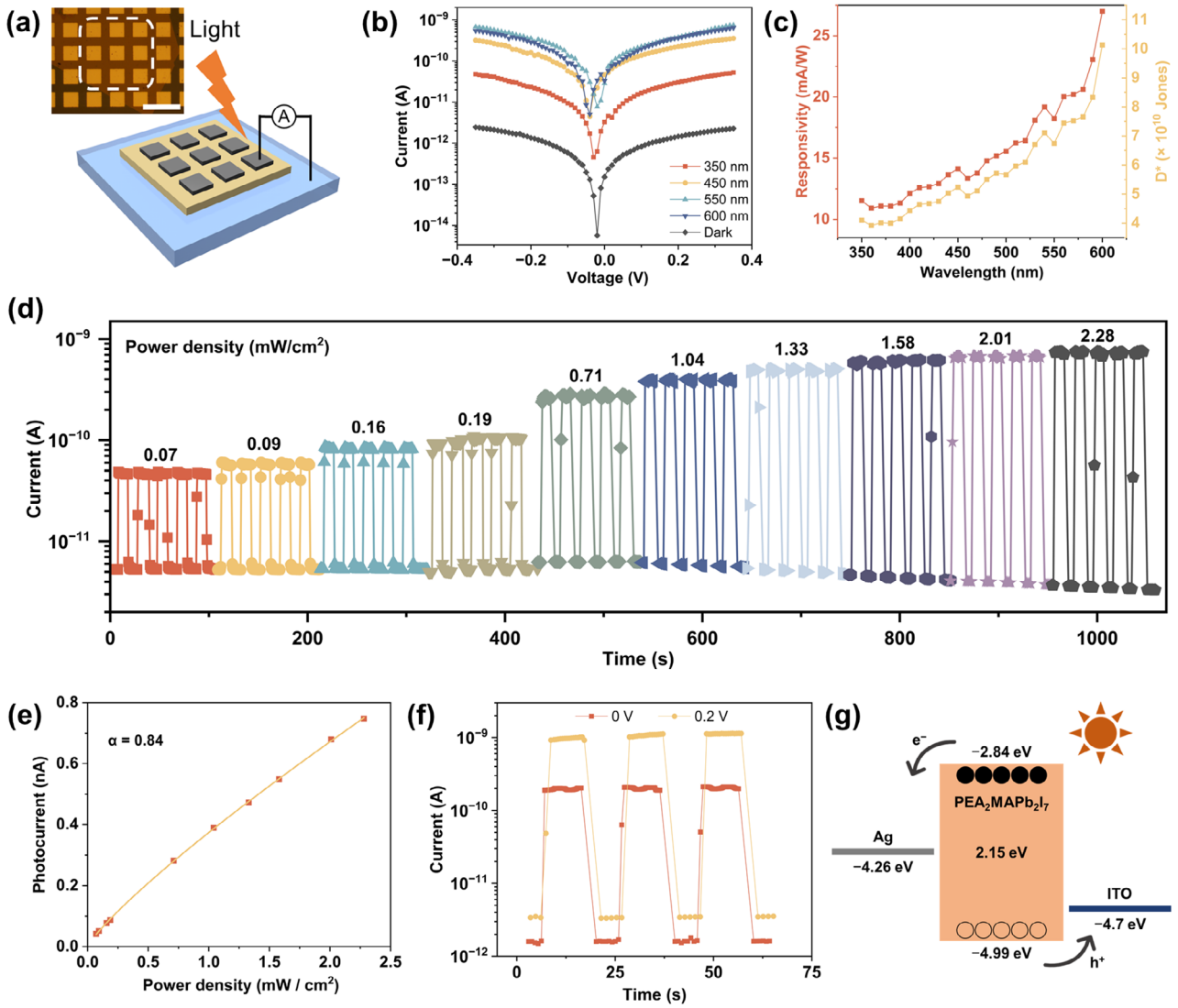

Figure 3. Optoelectronic properties of dual-functional devices. a) Schematic diagram of the device and corresponding optical image (inset). The white dashed box highlights a 3 × 3 array. Scale bar: 100 µm. b) *I–V* characteristics in the dark and under 350–600 nm illumination. c) R_λ and D^* of the device from 350 to 600 nm. d) *I–t* characteristics (at a 0.2 V bias) measured under different incident power densities and e) corresponding photocurrent as a function of light power density. f) *I–t* characteristics under 0 and 0.2 V bias. g) Band alignment diagram of the device.

which is consistent with the results of EDS mapping. Figure 2i shows the high-resolution XPS spectra of C 1s, N 1s, I 3d, and Pb 4f regions. The C 1s spectrum can be deconvoluted into three components located at 285.0 eV, 285.7 eV, and 286.9 eV, being assigned to C—C (sp^3) bond, aromatic C—C (sp^2) bond, and C—N^+ bond. The N 1s spectrum exhibits a single peak at 402.5 eV. The I 3d spectrum shows peaks at 630.9 and 619.4 eV, attributed to the characteristic doublet state $3d_{3/2}$ and $3d_{5/2}$ of I. The Pb 4f spectrum shows peaks at 143.7 eV and 138.8 eV, attributed to the characteristic doublet state $4f_{5/2}$ and $4f_{7/2}$ of Pb.

2.3. Optoelectronic Properties of Dual-functional Devices

The optoelectronic performance of the Ag/PMMA/$PEA_2MA_{n-1}Pb_nI_{3n+1}$/ITO ($n$ = 1–4) device is shown in **Figure 3**. Figure 3a presents the schematic diagram and working principle of the device, where optical stimuli are locally applied to a perovskite-based memristor array and the photocurrent is measured using a source meter. The exposed regions between adjacent Ag pads are ≈25 µm wide, which allows incident light to illuminate the perovskite layer. The inset shows an optical microscope image of the fabricated 3 × 3 array. As shown in Figure S11 and Table S1 (Supporting Information), the current-time (*I–t*) and current-voltage (*I–V*) characteristics of four devices (n = 1–4) demonstrate excellent optoelectronic responses. Among them, the device with n = 2 exhibits the lowest dark current, the highest on/off ratio, and the greatest detectivity, and is thus selected for further detailed study. Figure 3b shows the *I–V* characteristics of the device measured in the dark and under illumination from 350 to 600 nm, indicating a strong photocurrent response and broadband sensitivity with a

maximum on/off ratio of 328 and corresponding optimal response wavelength of 550 nm. The dark current remains at a minimum of ≈10^{-15} A, indicating excellent leakage suppression and low noise levels, which is crucial for achieving a high signal-to-noise ratio in low-light detection.[38] *I–t* characteristics under light illumination of broadband wavelength range further display the overall photoresponsivity of the photodetector. *I–t* curves under illumination from 350 to 600 nm are provided in Figure S12 (Supporting Information), confirming the broadband photocurrent response of the device. Responsivity (R_λ) and specific detectivity (D^*) are commonly used to evaluate the performance of the photodetector.[39] R_λ is defined as $R_\lambda = (I_l - I_d)/PA$, where I_l is the light current, I_d is the dark current, P is the incident power density, and A is the effective light area, reflecting the efficiency with which the photodetector converts light into electrical signals. D^* is calculated using $D^* = R_\lambda/(2eI_d/A)^{1/2}$, where $e = 1.6 \times 10^{-19}$ C, denoting the ability to detect weak signals in a noisy environment. As shown in Figure 3c, the device exhibits broadband photodetection capability from 350 to 600 nm. The R_λ and D^* both reach maximum values of 27.0 mA/W and 1.01×10^{11} Jones, respectively, at 600 nm, demonstrating the excellent performance in broadband response and array imaging. The *I–t* characteristics at a 0.2 V bias (Figure 3d) and *I–V* characteristics (Figure S13, Supporting Information) are measured under different light intensities, ranging from 0.07 to 2.28 mW cm^{-2} at 600 nm. The device exhibits clear and stable photocurrent responses with photocurrent rising progressively as the light intensity increases, indicating strong sensitivity and consistent performance. At higher optical power densities, a slight reduction in the baseline quasi-dark current between pulses is observed, attributed to light-induced filling or passivation of deep trap states that suppress leakage pathways and lower the apparent dark current.[40,41] The photocurrent of the device increases with the light intensity, which can be described by the power law formula ($I_{ph} = AP^\alpha$, $0.5 < \alpha < 1$),[42] where I_{ph} is defined as the photocurrent, A is a constant for a certain wavelength, and α is the exponent representing the photosensitivity linearity, depending on the processes of electron–hole generation, trapping, and recombination.[43] The fitting exponent α of 0.84 indicates a near-linear photocurrent response, demonstrating that the device is able to effectively detect light intensities over a broad range, exhibiting excellent optoelectronic performance(Figure 3e). Figure S14 (Supporting Information) shows the R_λ and D^* of the photodetector under various incident power densities, with both a peak responsivity of 39.1 mA/W and a detectivity of 1.15×10^{11} Jones observed at a power density of 0.07 mW cm^{-2}. The responsivity and specific detectivity reach their peaks at the lowest power density, since trap states dominate carrier dynamics, leading to prolonged carrier lifetimes and a nonlinear photocurrent response, thereby enhancing responsivity.[44] When light intensity exceeds 0.5 mW cm^{-2}, both responsivity and detectivity decrease and remain stable as the intensity increases further. The *I–t* characteristics of the device under 0 and 0.2 V bias exhibit prompt and regular rectangular photocurrent responses with excellent cycling stability. A current on/off ratio of up to two orders of magnitude is observed at both 0 and 0.2 V bias (Figure 3f). At a 0 V bias, carrier transport and photocurrent generation are driven by the built-in electric field present in the device.[45] As illustrated in Figure 3g, the device operates in a self-powered mode at zero bias as a Schottky-type photodiode, enabled by the built-in electric field resulting from the asymmetric contact structure.[41,46] Since lead halide perovskites are typically n-type, electron transport dominates the photocurrent generation.[47] Under illumination, photogenerated carriers are efficiently separated and collected by the electrodes, which enables a photocurrent output without any external bias.[48,49] Figure S15 (Supporting Information) demonstrates the long-term stability of the photocurrent under repeated light on/off cycles over 1200 s with 550 nm illumination. The device maintains consistent and stable photocurrent amplitudes throughout the test duration, with the on/off ratio after the final cycle remaining above 90% of the initial value.

2.4. Stable and Energy-Efficient Resistive Switching of the Memristor

The memristive performance of the Ag/PMMA/$PEA_2MAPb_2I_7$/ITO device is shown in **Figure 4**. The *I–V* curves under multiple cycles are shown in Figure 4a, with the voltage swept in the sequence of −1.0 V → 0 V → 1.0 V → 0 V → −1.0 V. As the voltage increases toward the setting voltage (V_{set}, ≈0.5 V), the memristor switches from HRS to LRS with an on/off ratio up to ≈5×10^5. Subsequently, as the voltage is swept in the negative direction, the LRS remains unchanged. Only when the applied voltage decreases below the reset voltage (V_{reset}) does the device return to the original HRS and remain in this state for the rest of the negative voltage sweep, displaying a typical unipolar resistive switching cycle. Notably, the device exhibits forming-free resistive switching, owing to the low activation energy for ion migration and the mobility of iodine vacancies and interstitials in the hybrid perovskite.[50] Every fifth cycle from cycle 5 to cycle 60 is displayed, confirming stable resistive switching behavior with an average V_{set} of 0.44 V. The setting power consumption (P_{set}) is a key indicator of energy efficiency in memory applications, defined as $P_{set} = V_{set} \times I_{set}$,[51] where I_{set} denotes the current corresponding to V_{set}. Notably, the fabricated memristor exhibits a remarkably low setting power of ≈1.21 pW, enabling energy-efficient applications. As shown in Figure S16 and Table S2 (Supporting Information), the $n = 2$ memristor demonstrates clear advantages over devices based on $n = 1$, 3, and 4, including the lowest switching current, highest on/off ratio, and lowest power consumption, highlighting its superior suitability for high-performance and energy-efficient memory applications. Figure 4b shows the endurance performance of the memristor over 100 consecutive switching cycles. The LRS current remains ≈10^{-5} A during the first 75 cycles with a slight decline to ≈10^{-6} A near the end, while the HRS current stays stable at ≈10^{-12} A. Furthermore, the device is immune to read-disturb, showing no observable degradation after 1.6×10^4 s under a 0.2 V read bias. Throughout the measurement, the stable on/off ratio over six orders of magnitude confirms excellent memory retention (Figure 4c). Compared with recently reported memristors based on metal oxides, chalcogenides, 2D materials, and other perovskites, the Ag/PMMA/$PEA_2MAPb_2I_7$/ITO device achieves both ultra-low power consumption and a high on/off ratio, which are essential for preprogrammed systems and secure hardware applications, as shown in Figure 4d and Table S3

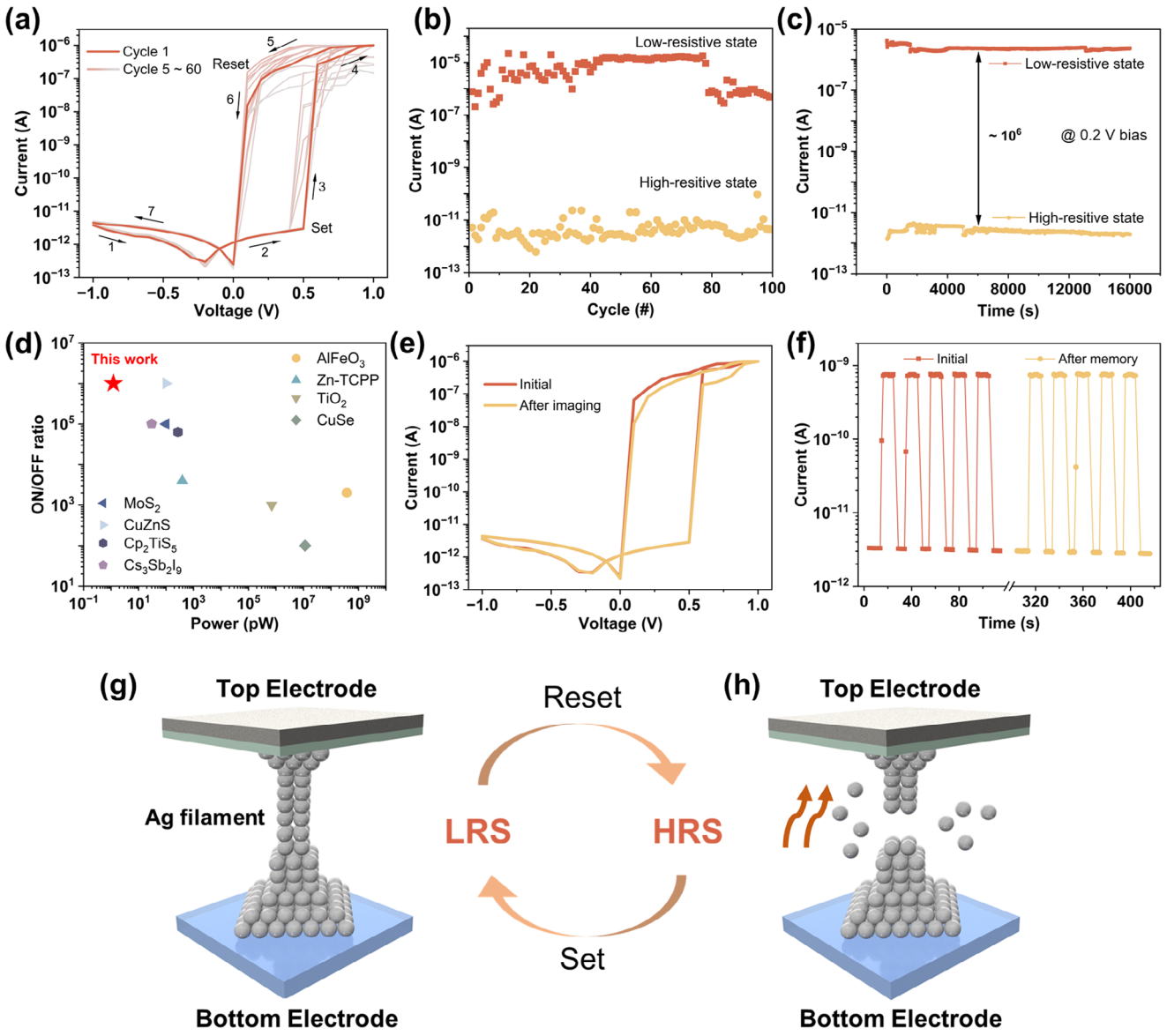

Figure 4. Stable and energy-efficient resistive switching of the memristor. a) *I–V* curves of the device at cycle 1 and every fifth cycle from cycle 5 to cycle 60. b) Endurance characteristics measured over 100 switching cycles. c) Retention performance over time. d) Comparison of the on/off ratio and power consumption of this device with those reported in the literature. e) *I–V* curves of the device before and after imaging. f) *I–t* curves of the device before and after memory operation. g–h) Schematic illustration of the resistive switching mechanism: g) LRS and h) HRS.

(Supporting Information). The mutual independence of the device's dual functionalities is demonstrated in Figure 4e,f. After repeated photocurrent response cycles, the memristive *I–V* characteristics remain stable with clear switching thresholds. Similarly, the photocurrent–time response retains sharp transitions and a stable on/off ratio after multiple resistive switching cycles, demonstrating functional repeatability and reusability.

The resistive switching behavior of the device is attributed to the formation and rupture of Ag filaments, as illustrated in Figure 4g,h.[52–54] When a positive voltage is applied, Ag atoms at the top electrode are oxidized into Ag^+ ions ($Ag \rightarrow Ag^+ + e^-$) and migrate through the perovskite layer and reach the bottom ITO layer, where they are reduced back to Ag atoms. Upon further accumulation, the Ag atoms form a conductive filament between the top and bottom electrodes, thus switching the device from HRS to LRS. Once the external field is removed, the filament is energetically and kinetically pinned by interfacial adhesion and the high activation barrier for the back diffusion of Ag^+.[55] As a result, the low-resistance path persists without any power supply. The Ag filament stays intact when the applied voltage is swept negatively until the voltage drops below the reset threshold (V_{reset}). Once the voltage falls below V_{reset}, the persistent current results in a highly localized Joule heating effect, which significantly increases the temperature at the narrowest region of the filament. The thermal stress facilitates the partial dissolution or rupture of the Ag filament, as Ag atoms

or ions are driven back toward the top Ag electrode.[56] Consequently, the continuous conductive pathway is disrupted, causing the device to revert to its original HRS. To further confirm the resistive switching mechanism, control devices with inert Au top electrodes (Au/PMMA/$PEA_2MAPb_2I_7$/ITO) were fabricated. As shown in Figure S17 (Supporting Information), no resistive switching behavior was observed in these Au-based devices under bias up to ±2 V, indicating that Ag migration is essential for the observed switching characteristics.

2.5. Ternary-State Key Programming for Reconfigurable Security Monitoring

By integrating optical sensing with electrical memory programming in a single device architecture, multi-level current states are achieved for logic operations and security applications, as demonstrated in **Figure 5**. Figure 5a–c illustrates the working mechanism and different output current (I_{out}) of the device under different input conditions monitored at a read bias of 0.2 V. The 2D map in Figure 5b enables direct, quantitative comparison of the absolute current levels for each logic state, whereas the 3D rendering in Figure 5c visualizes the same dataset to emphasize the spatial distribution and clear state separation across the array. The initial HRS in the absence of any stimulation corresponds to logic "0," with an I_{out} of $\approx 10^{-12}$ A. Under an event-driven optical input (600 nm, 2.28 mW cm^{-2}), the device current rises to $\approx 10^{-9}$ A upon light exposure, representing logic "1." When a positive electrical pulse of +0.5 V for 5 ms is applied, the device undergoes a resistive switching transition into the LRS with an I_{out} of $\approx 10^{-6}$ A, representing logic "2." To further confirm the reliability of multilevel switching, statistical analysis of the three logic current states across 25 devices reveals well-separated distributions with minimal overlap, ensuring clear noise margins and high reproducibility (shown in Figures S18 and S19 and Table S4, Supporting Information). Based on the measured setting power of ≈1.21 pW, the write energy per cell is calculated as $E_{unit} = P_{set} \times t = 6.05$ fJ. Since each ternary memory state contains $\log_2(3)$ bits of information, the write energy per bit for this device is ≈3.8 fJ/bit, underscoring the remarkably low energy consumption achieved with ternary memory encoding (see Note S1, Supporting Information). The initial current of a 3 × 3 device array, along with the corresponding 2D current distribution, is presented in Figure S20 (Supporting Information). Figure 5d presents the operation flow of the dual-factor access system. During permission activation, a specific pattern is electrically programmed into the 3 × 3 array by switching the states of targeted cells. The resulting 2D map clearly presents the static access code, with logic state "2" pixels standing out from the logic state "0" background. In the entry verification step, the card is presented to the access terminal for electrical readout. Each user possesses a unique electrically programmed access pattern, which serves as an individualized identity code. Access is granted only when the measured logic map exactly matches the stored template, ensuring reliable user authentication. During instrument usage, the card is inserted into the corresponding instrument slot, each of which contains a built-in light source that projects a distinct optical pattern onto the array. These optical patterns and their activation positions are unique to each instrument, enabling device-specific access control and continuous monitoring of user activity. Exposure to the patterned illumination yields a corresponding 2D logic map in which pixels illuminated by light are assigned logic state "1," electrically programmed sites retain logic state "2," and all other pixels remain at logic state "0." This unique combination of optical and electrical logic states acts as a real-time identifier, clearly indicating which specific user is operating which instrument at any given moment. The resulting spatially resolved logic states enable dynamic and real-time visualization of both user presence and instrument operation. When the user leaves and the card is removed, the optical input ceases, and all pixels return to their initial "0" states. The static pattern can also be readily erased and rewritten through electrical operations. For example, after erasing a previously programmed "I" pattern, a new "X" pattern can be electrically written, allowing for flexible rewriting of static access codes when necessary (Figure S21, Supporting Information). Figure 5e shows the 3D current maps for each stage, highlighting the excellent separation and recognition of the different device states and enabling robust dual-factor access and real-time monitoring. Beyond the 3 × 3 array demonstration, larger arrays are readily achievable. The largest nanoplates we synthesized are capable of supporting up to a 6 × 4 (24-pixel) electrode array (Figure S22, Supporting Information), demonstrating clear scalability.

Compared to conventional hardware systems that rely solely on either optical or electrical mechanisms, this work integrates both modalities as dual inputs, enabling flexible, real-time management and supporting dynamic monitoring of user and device status. Optical programming provides a volatile, non-contact channel for defining intermediate logic states, allowing targeted activation without additional wiring, and inherently self-erasing upon removal of illumination to prevent unintended data persistence. The ternary logic structure substantially enhances the information capacity, expanding the number of state configurations from $2^9 = 512$ to $3^9 = 19{,}683$ in a 3 × 3 array. Furthermore, each logic state is directly associated with a physically distinct current level determined by optical and electrical inputs, allowing for clear state recognition and straightforward data readout without the need for additional encoding or post-processing. The integration of dual memory modalities, enhanced information density, and intrinsic self-erasure endows the device with unique advantages for secure, reconfigurable, and real-time hardware access management.

3. Conclusion

In conclusion, we synthesized high-quality $PEA_2MA_{n-1}Pb_nI_{3n+1}$ hybrid perovskite nanoplates with excellent uniformity and crystallinity. Utilizing these nanoplates, we fabricated an Ag/PMMA/$PEA_2MAPb_2I_7$/ITO optoelectronic memristor capable of broadband self-powered photodetection and reliable resistive switching, offering a compact and versatile platform for hardware-level access control and security monitoring. As a photodetector, the device displays a high responsivity of 39.1 mA/W and a high detectivity of 1.15×10^{11} Jones. As a memristor, it exhibits a low operating voltage of 0.44 V, an ultra-low setting power of ≈1.21 pW, an ultra-high on/off ratio of 10^6, stable cyclic endurance over 100 cycles, and a long programmable retention time of over 1.6×10^4 s. The implementation of ternary logic

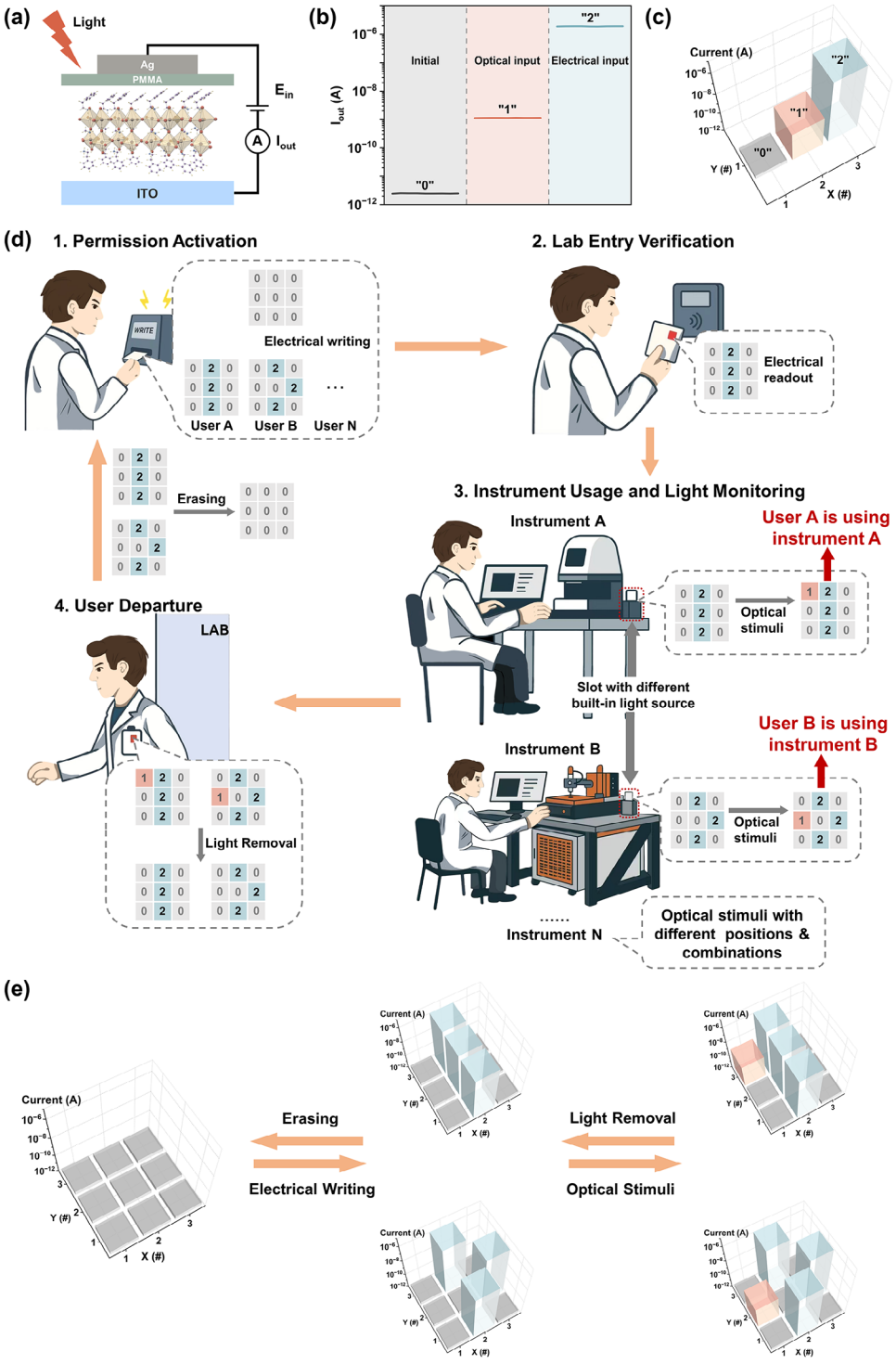

Figure 5. Ternary-state key programming for reconfigurable security monitoring. a) Working mechanism of the dual-functional device. b) I_{out} among initial state, under optical input (2.28 mW cm^{-2}, 600 nm) and electrical input (+0.5 V, 5 ms). c) 3D current map for different states. d) Practical operation flow and corresponding 2D maps: 1. Permission activation by electrical writing; 2. Lab entry verification via card readout; 3. Real-time instrument monitoring enabled by slot-specific optical stimulation; 4. User departure upon light removal. e) Representative 3D current maps of the device array during the entire operation cycle.

encoding enables high information density and clear current-level separation, supporting robust, real-time dual-factor access management with an ultra-low write energy of ≈3.8 fJ/bit. By eliminating the need for additional encoding or complex mapping, this platform supports secure hardware applications and paves the way for energy-efficient artificial vision, multivalued logic operations, in-memory sensory processing, and other advanced technologies.

4. Experimental Section

Reagents: PEAI (99.9%), MAI (99.9%), PbI_2 (≥98.0%) were purchased from Advanced Election Technology Co., Ltd. Hydroiodic acid (HI, 55.0–58.0% in H_2O, contains ≤1.5% H_3PO_2), poly(methyl methacrylate) (PMMA), and chlorobenzene (99.8%, anhydrous) were purchased from Sinopharm. All of the reagents were used as received without further treatment.

Growth of Hybrid Nanoplates: Taking $PEA_2MAPb_2I_7$ ($n = 2$) as an example, the solution was prepared by dissolving 16.6 mg PEAI (0.067 mmol), 122.2 mg MAI (0.77 mmol), and 184.4 mg PbI_2 (0.40 mmol) into 2.5 mL aqueous HI. Then, the solution was heated to 130 °C with constant magnetic stirring for 2 h. The preparation procedures for PEA_2PbI_4, $PEA_2MA_2Pb_3I_{10}$, and $PEA_2MA_3Pb_4I_{13}$ solutions were identical, except for the molar ratios of PEAI, MAI, and PbI_2, which are summarized in Table S5 (Supporting Information). The resulting solution was stored in a drying oven at 70 °C for further use. In ambient conditions, 5 µL of the precursor solution was dropped onto a hydrophobic glass substrate using a micropipette. As the temperature decreased, the solution became saturated and precipitated perovskite on the surface.

Construction of Devices: The dual-functional devices were constructed in a vacuum glove box with the help of an accurate transfer platform (METATEST, E1-T). The perovskite nanoplates were separated using polydimethylsiloxane (PDMS). PDMS was gently pressed onto the surface for a few seconds, allowing the floating nanoplates to transfer onto the PDMS without mechanical damage. The glass slide with PDMS was affixed onto the sample stage, while the indium tin oxide (ITO) substrate was affixed on the lower stage by vacuum pump. After the transfer of perovskite nanoplates, a PMMA solution in chlorobenzene (5 mg mL^{-1}) was spin-coated at 5000 rpm and subsequently annealed at 85 °C for 10 min. Then, the Ag electrodes (100 nm) were thermally evaporated onto the sample by putting Ni grids (400 meshes, with square voids of 37 µm side size) as a shadow mask. After removal of the Ni grids, square-shaped electrodes with a spacing of ≈25 µm were successfully formed on the perovskite nanoplates.

Characterization and Performance Testing: Atomic-force microscope (AFM, Bruker Dimension Edge) was applied to measure the height and roughness data of the samples. Transmission electron microscope (TEM, JEOL JEM-F200), high-resolution TEM (HRTEM), and selected area electron diffraction (SAED) were used to characterize the crystal structure. Scanning electron microscope (SEM, ZEISS Sigma 300) and energy dispersive X-ray spectroscopy (EDS) mapping were used to investigate the surface morphology and element distribution, and the basic structure was observed by optical microscopy (Olympus). The structural characterization of the nanosheets was characterized by a Bruker D8 Advance X-ray diffractometer (XRD, Cu-K_α radiation source, $\lambda = 1.5406$ Å). X-ray photoelectron spectroscopy (XPS) spectra were obtained by using ULVAC-PHI GENESIS with Al K_α (energy = 1486.6 eV, voltage = 15 kV, beam current = 10 mA). Photoluminescence (PL) spectroscopy was performed using a Renishaw inVia Qontor system with excitation lasers at 325 nm and 532 nm to evaluate the bandgap and infer the crystallinity of the nanosheets. The dual-functional device was performed by a semiconductor analyzer (Keithley 4200-SCS) connected to a 75 W Xe lamp equipped with a monochromator as the light source. For *I–t* measurements, the device was illuminated in repeated cycles of 10 s on and 10 s off (20-s period, 0.05 Hz). A NOVA II power meter (Ophir Photonics) was used to measure the illumination intensity. All the measurements were tested at room temperature.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

dual-functional device, hybrid perovskites, low-power, optoelectronic memristors, security monitoring

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